HydraX SM Optical Transceiver Module
MPO QSFP-DD PAM4 400G DR4 1310nm 500m

Aggredation Mode 400GBASE-DR4 compliant 4× 53.125Gbd PAM4 and 400GAUI-8 compliant 8 ×26.5625 Gbd PAM4

Breakout Mode 4×100GBASE-DR compliant 53.125GBd PAM4 and 100GAUI-2 compliant 2× 26.5625 Gbd PAM4

QSFP-DD MSA compliant

MPO-12 connector with APC end face

Hot Pluggable

Power consumption < 12W

CMIS 4.0 management interface

Design Refernce
IEEE 802.3-2018
IEC 60825 Class 1

Application
400GBASE DR4 Proprietary
High Speed Interconnections
Data center 400G SM link

Working Condition
Operation Temperature
-0℃ ~ +70℃ (Case)
Storage Temperature
-40℃ ~ +85℃ (Ambient)
Relative humidity
5% ~ 95%

Compliance
CE Mark
FCC Mark

Safety and EMI
Protection of over voltage/current

General Description
The Hermesys HydraX™ series QDD-21400005DR4X5 400G QSFP-DD DR4 hot pluggable optical transceiver is a high performance solution for 400GE links for up to 500 m over single mode fiber (SMF) with MPO-12 connector. It combines 8x 26.5625GBd PAM4 electrical lanes into 4x 53.125 GBd PAM4 optical channels in compliance with IEEE 400GBASE-DR4. Superior performance and reliability is achieved through advanced transmitter and receiver design using cooled 4x EA-DFB-LDs and 4x PIN PDs.

Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	V_{CC}	0		3.6	V	
Optical Receiver Input	V_{in}			+5.0	dBm	Average each lane

Hermesys

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Supply Voltage Noise Tolerance	PSNR	-	-	66	mV	10 Hz –10 MHz
Power Consumption	P_6	-	-	12	W	
Instantaneous peak current	Icc_ip_6			4800	mA	
Sustained peak current	Icc-sp_6			3960	mA	
Supply Current	Icc-6	--	-	3827.8	mA	Steady state
Case Temperature	TC	0	25	70	°C	

Electrical Characteristics

Parameter	Min	Typ	Max	Unit	Notes
Module output (each lane, at TP4) [Note 1]					
Signaling rate per lane (range)	-100ppm	26.5625	+100ppn	GBd	
AC Common-mode output voltage (RMS)	-		17.5	mV	
Differential peak-to-peak output voltage	-		900	mV	
Near-end ESMW (Eye symmetry mask width)	0.265		-	UI	
Near-end Eye height, differential	70			mV	
Far-end ESMW (Eye symmetry mask width)	0.2		-	UI	
Far-end Eye height, differential	30		-	mV	
Far-end pre-cursor ISI ratio	-4.5		2.5	%	
Differential output return loss	Equation (83E-2)		-	dB	Note 2
Common to differential mode conversion return loss	Equation (83E-3)		-	dB	Note 2
Differential termination mismatch	-		10	%	
Transition time (20% to 80%)	9.5		-	ps	
DC common mode voltage	-350		2850	mV	
Module input (each lane)					
Signaling rate per lane (range)	100ppm	26.5625	+100ppm	GBd	Note 2
Differential pk-pk input voltage tolerance	900	-	-	mV	
Differential input return loss	Equation (83E-5)	-	-	dB	
Differential to common mode input return loss	Equation (83E-6)	-	-	dB	
Differential termination mismatch	-	-	10	%	

ESMW (Eye symmetry mask width)	0.22	0.22	+100ppm	UI	Note 2
Eye width	0.22	0.22	-	UI	
Applied pk-pk sinusoidal jitter	Table 120E-6			MHz, UI	
Eye height	32		-	mV	
Single-ended input voltage tolerance	-0.4		3.3	V	
DC common mode voltage	-350		2850	mV	

Note 1: Electrical module output is squelched for loss of optical input signal
Note2: IEEE Std 802.3-2018 Section 6

Optical Characteristics

Receiver Optical Characteristics						
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Channel data rate	f_{DC}		106.25		Gb/s	
Signaling rate	f_{SG}		53.125		GBd	PAM4
Signal speed variation from nominal	Δf_{SG}	-100		+100	ppm	
Lane wavelength (range)	λ_C	1304.5		1317.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Average launch power, each lane		-2.9		4.0	dBm	Note1
Outer Optical Modulation Amplitude (OMAouter), each lane		-0.8		4.2	dBm	Note2
Launch power in OMAouter minus TDECQ, each lane		-2.2			dBm	
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.4	dB	
Average Optical Output Power of Off Transmitter, each lane	Poff					
Extinction Ratio, each lane	ER	3.5			dB	
RIN21.4OMA				-136	dB/Hz	
Optical return loss tolerance				21.4	dB	
Transmitter reflectance				-26	dB	Note 3
Average receive power, each lane		–5.9		4.0	dBm	Note 4
Receive power (OMAouter), each lane				4.2	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane		Max (-3.9, SECQ - 5.3), [Figure 3]				Note 5,6
Stressed receiver sensitivity (OMAouter), each lane				-1.9	dBm	Note 5, 7
Conditions of stressed receiver sensitivity test [Note 8]						
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ		3.4		dB	
OMAouter of each aggressor lane			4.2		dBm	

Note 1: Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
Note 2: Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed these values.

Note 3: Transmitter reflectance is defined looking into the transmitter.
Note 4: Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
Note 5: For when Pre-FEC BER is 2.4 x 10-4 .
Note 6: Receiver sensitivity (OMAouter), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB.
Note 7: Measured with conformance test signal at TP3 (see IEEE Std 802.3-2018 section 8 clause 124.8.9) for the BER specified in IEEE Std 802.3-2018 section 8 124.1.1.
Note 8: These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

RX_LOS Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Receiver Loss of Signal Indicator Assert Level	RX_LOS	-15	-	-7.9	dBm	Average power
Receiver Loss of Signal Indicator De-assert Level		-	-	-7.4	dBm	Average power
Hysteresis		0.5			dB	

HIGH SPEED DATA INTERFACE

Rx(n)(p/n)
Rx(n)(p/n) are QSFP-DD module receiver data outputs. Rx(n)(p/n) are AC-coupled 100 Ohm differential lines that should be terminated with 100 Ohm differentially at the Host ASIC. The QSFP-DD module host interface is internally AC coupled, so AC-coupling is not required on the host PCB.
Output squelch for loss of optical input signal (RX Squelch) is required and shall function as follows. In the event of the Rx input signal on any optical port becoming equal to or less than the level required to assert LOS, the receiver output(s) associated with that Rx port shall be squelched. A single Rx optical port can be associated with more than one Rx output. In the squelched state, output impedance levels are maintained, while the differential voltage amplitude shall be less than 50 mVpp.

Tx(n)(p/n)
Tx(n)(p/n) are QSFP-DD module transmitter data inputs. They are AC-coupled 100 Ohm differential lines with 100 Ohm differential terminations inside the QSFP-DD optical module. The AC coupling is implemented inside the QSFP-DD optical module and not required on the Host board.
Output squelch for loss of electrical signal (Tx Squelch) is an optional function. Where implemented, it shall function as follows. In the event of the differential, peak-to-peak electrical signal amplitude on any electrical input channel becoming less than 70 mVpp, then the transmitter optical output associated with that electrical input channel shall be squelched and the associated TxLOS flag set. If multiple electrical input channels are associated with the same optical output channel, the loss of any of the incoming electrical input channels causes the optical output channel to be squelched.
For applications, e.g. Ethernet, where the transmitter off condition is defined in terms of average power, squelching by disabling the transmitter is recommended and for applications, e.g. InfiniBand, where the transmitter off condition is defined in terms of OMA, squelching the transmitter by setting the OMA to a low level is recommended.

Control Interface

Low Speed Control Pins

In addition to the 2-wire serial interface the transceiver has the following low speed signals for control and status: LPMode, ResetL, ModSel, IntL and ModPrsL. See the QSFP-DD MSA Hardware Specification for detailed descriptions of each signal.

Low Speed Electrical Specifications

Low speed signaling other than SCL and SDA is based on Low Voltage TTL (LVTTL) operating at Vcc

Low Speed Control and Sense Signals

Parameter	Symbol	Min.	Max.	Unit	Remarks
SCL and SDA	VOL	0	0.4	V	IOL(max)=3 mA for fast mode, 20 mA for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	Vcc*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use MAX 3.0 kohm pull-up resistor. For 1000 kHz clock rate refer to Figure 45 in QSFPDD MSA HW Spec [3].
	Cb		200	pF	For 400 kHz clock rate use MAX 1.6 kohm pullup resistor. For 1000 kHz clock rate refer to Figure 45 in QSFPDD MSA HW Spec [3].
LPMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	Vcc+0.3	V	
	|Iin|		360	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0 mA
	VOH	Vcc-0.5	Vcc+0.3	V	10 kohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL= 2.0mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

2-Wire Management Interface

A management interface, as already commonly used in other form factors like QSFP, SFP, and CDFP, is specified in order to enable flexible use of the module by the user. This QSFP-DD specification is based on SFF-8636 but with modifications to support an 8-channel module, and as such is not directly backwards compatible with SFF-8636. Byte 00 on the Lower Page or Address 128 Page 0 is used to indicate the use of the QSFP-DD memory map rather than the QSFP memory map.

The QSFP-DD Module supports alarm, control and monitor functions via a two-wire interface bus. Upon module initialization, these functions are available. QSFP-DD two-wire electrical interface consists of 2 pins of SCL (2-wire serial interface clock) and SDA (2-wir serial interface data). The low speed signaling is based on Low Voltage CMOS (LVCMOS) operating at Vcc. Hosts shall use a pull-up resistor connected to Vcc_host on the 2-wire interface SCL (clock) and SDA (Data) signals. The timing requirements on the two- wir interface are listed in Table 7 and Figure 4.

Management Interface Timing

Parameter	Symbol	Min.	Max.	Unit	Remarks
		Fast Mode Plus (1 MHz)			
Clock Frequency	fSCL	0	1000	kHz	
Clock Pulse Width Low	tLOW	0.50		µs	
Clock Pulse Width High	tHIGH	0.26		µs	
Time bus free before new transmission can start	tBUF	1		µs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.26		µs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.26		µs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		µs	
Data In Setup Time	tSU.DAT	0.1		µs	
Input Rise Time	tR		120	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		120	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.26		µs	
STOP Hold Time	tHD.STO	0.26		us	
Aborted sequence bus release	Deselect _Abort		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP-DD module releasing SCL and SDA
ModSelL Setup Time1	tSU.Mod SelL	2		ms	ModSelL Setup Time is the setup time on the select lines before the start of a host initiated serial bus sequence.
ModSelL Hold Time1	tHD.Mod SelL	2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module Select status.
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_ hold		500	us	Maximum time the QSFP-DD module may hold the SCL line low before continuing with a read or write operation
Complete Single or Sequential Write to non- volatile registers	tWR		80	ms	Complete Write of up to 8 Bytes
Accept a single or sequential write to volatile memory.	tNACK		80	ms	Time required for the module to accept a single or sequential write to volatile memory.
Endurance (Write Cycles)		50k			Module Case Temperature= 70 °C

Note 1: When the host has determined that module is QSFP-DD, the management registers can be read to determine alternate supported ModSelL set up and hold times.

Soft Control and Status Functions

Below lists the required timing performance for software control and status functions

Parameter	Symbol	Min.	Max.	Unit	Remarks
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on1 , hot plug or rising edge of reset until completion of the MgmtInit State
ResetL Assert Time	t_reset_init	10		µs	Minimum pulse time on the ResetL signal to initiate a module reset.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol
IntL Deassert Time	toff_IntL		500	µs	Time from clear on read2 operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		100	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntL asserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)3 until associated IntLassertion is inhibited
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)3 until associated IntL operation resumes

Note 1: Power on is defined as the instant when supply voltages reach and remain at or above the minimum level
Note 2: Measured from the rising edge of SDA in the stop bit of the read transaction.
Note 3: Measured from the rising edge of SDA in the stop bit of the write transaction
Note 4: Rx LOS condition is defined at the optical input by the relevant standard.

Squelch and Disable Assert/De-assert and Enable/Disable Timing

I/O Timing for Squelch & Disable

Parameter	Symbol	Min.	Max.	Unit	Remarks
Rx Squelch Assert Time	ton_Rxsq		15	ms	Time from loss of Rx input signal until the squelched output condition is reached.
Rx Squelch De- assert Time	toff_Rxsq		5000 (Tentative)	ms	Time from resumption of Rx input signals until normal Rx output condition is reached.
Tx Squelch Assert Time	ton_Txsq		400	ms	Time from loss of Tx input signal until the squelched output condition is reached.
Tx Squelch De-assert Time	toff_Txsq		5000 (Tentative)	ms	Time from resumption of Tx input signals until normal Tx output condition is reached.

Tx Disable Assert Time	ton_txdis		100	ms	Time from the stop condition of the Tx Disable write sequence 1 until optical output falls below 10% of nominal
Tx Disable Assert Time (optional fast mode)	ton_txdisf		3	ms	Time from Tx Disable bit set (value = 1b)1 until optical output falls below 10% of nominal
Tx Disable De-assert Time	toff_txdis		400	ms	Time from Tx Disable bit cleared (value = 0b)1 until optical output rises above 90% of nominal
Tx Disable De-assert Time (optional fastmode)	toff_txdisf		10	ms	Time from Tx Disable bit cleared (value = 0b)1 until optical output rises above 90% of nominal
Rx Output Disable Assert Time	ton_rxdis		100	ms	Time from Rx Output Disable bit set (value = 1b)1 until Rx output falls below 10% of nominal
Rx Output Disable De-assert Time	toff_rxdis		100	ms	Time from Rx Output Disable bit cleared (value = 0b)1 until Rx output rises above 90% of nominal
Squelch Disable Assert Time	ton_sqdis		Not applicable (Tx/Rx Auto Squelch Disable not supported)		This applies to Rx and Tx Squelch and isthe time from bit set (value = 0b)1 until squelch functionality is disabled.
Squelch Disable De-assert Time	toff_sqdis		Not applicable (Tx/Rx Auto Squelch Disable not supported)		This applies to Rx and Tx Squelch and isthe time from bit cleared (value = 0b)1 until squelch functionality is enabled

Note 1: Measured from LOW to HIGH SDA signal transition of the STOP condition of the write transaction.

Power

The power supply has six designated pins, VccTx, VccTx1, Vcc1, Vcc2, VccRx, VccRx1 in the connector. Vcc1 and Vcc2 are used to supplement VccTx, VccTx1, VccRx or VccRx1 at the discretion of the module vendor. Power is applied concurrently to these pins.

A host board together with the QSFP-DD module(s) forms an integrated power system. The host supplies stable power to the module. The module limits electrical noise coupled back into the host system and limits inrush charge/current during hot plug insertion.

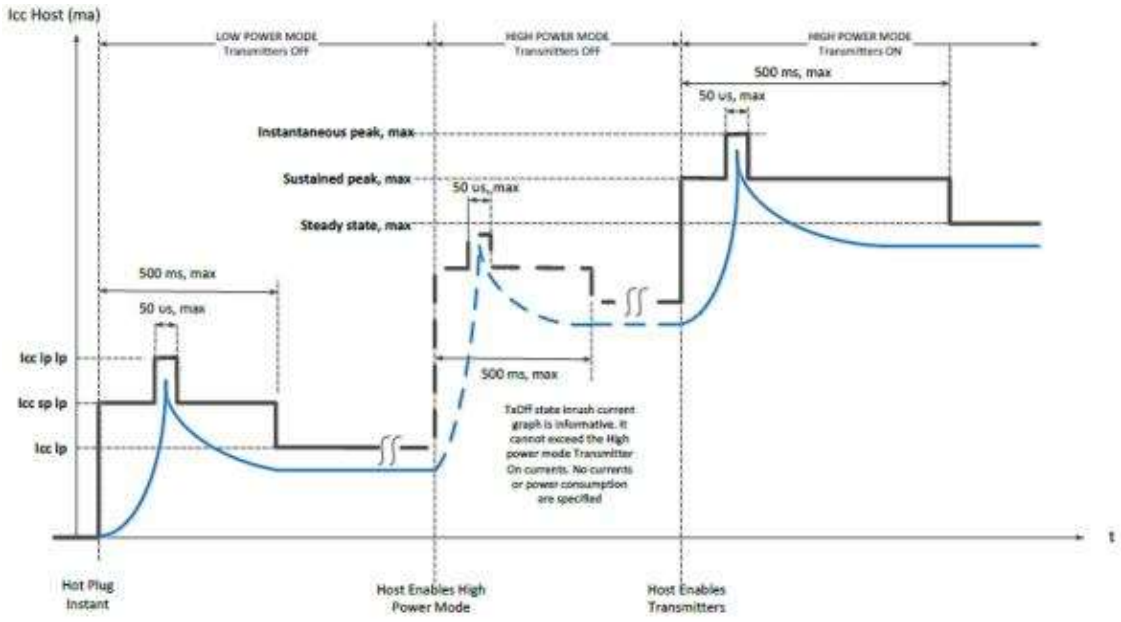
All power supply requirements in Table 2 shall be met at the maximum power supply current. No power sequencing of the power supply is required of the host system since the module sequences the contacts in the order of ground, supply and signals during insertion.

Maximum Power Classes

Power Class	Max Power (W)
1	1.5
2	3.5
3	7.0
4	8.0
5	10
6	12
7	14
8	>14

Module Power Supply Specification

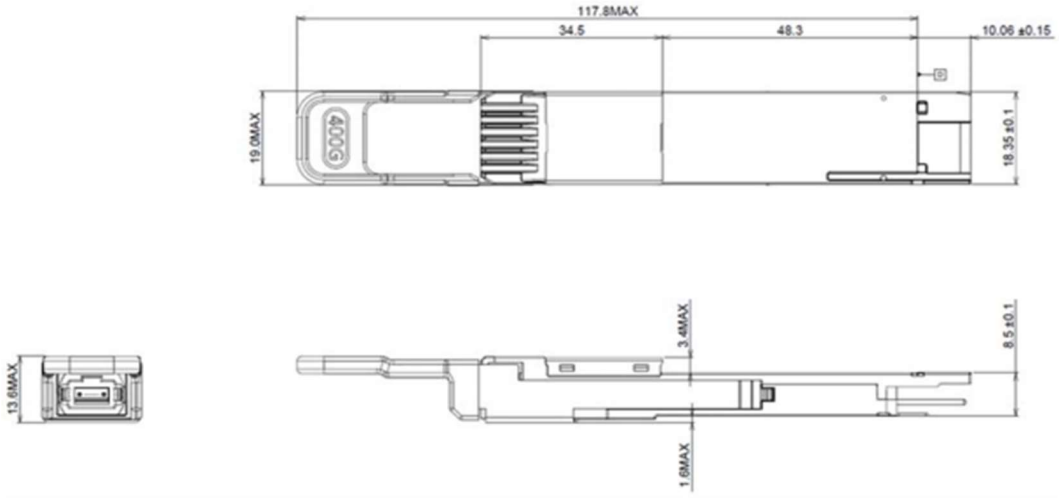
In order to avoid exceeding the host system power capacity, upon hot-plug, power cycle or reset, all QSFP- DD modules shall power up in Low Power Mode if LPMode is asserted. If LPMode is not asserted, the module will proceed to High Power Mode without host intervention. Below shows waveforms for maximum instantaneous, sustained and steady state currents for Low Power and High Power modes.

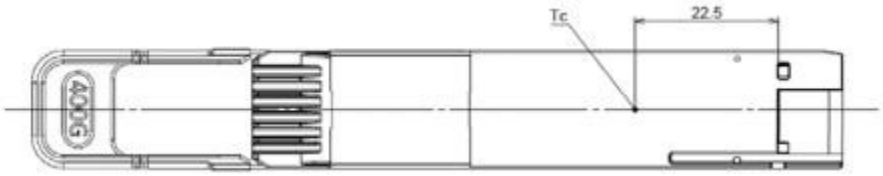


Instantaneous and Sustained Peak Currents for Icc Host

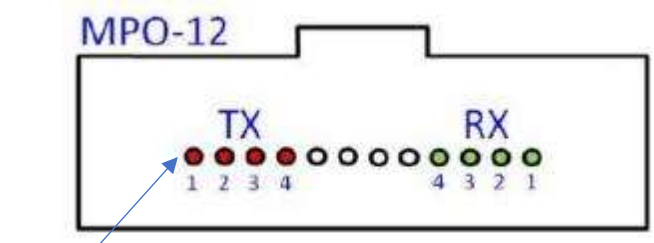
Dimension of Case

Unit:mm





Case temperature measurement point



APC end face

Looking into the connector, transmitter is on the left.

Order Information

Part Number	Grade	Packing info
QDD-21400005DR4X5	Commercial -0~70 °C	400 pcs per carton (10pcs per tray, 10 tray per inner box, 4 inner box per carton)

Note:
X means compatible equipment code.

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